AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 2, line 19, with the following rewritten paragraph:

FIG. 3 shows a further conventional type stack package 800. Referring to FIG. 3, the stack package 800 comprises a plurality of fan-out type chip scale packages 810 and a conventional ball grid array (BGA) type chip scale package 805. The fan-out type chip scale packages 810 are electrically connected to each other and to the BGA chip scale package 805 with solder balls 838 formed on a lower surface of substrate 821. The BGA type chip scale package 805 is stacked at the lowest level. The solder balls 837 are formed on the entire area of the BGA type chip scale package, and function as Input/Output ports of the stack package 800. This kind of stack package has the same technical drawback, i.e., the difficulty of standardizing the solder ball arrangement, as that of the stack package 600.

Please replace the paragraph beginning on page 5, line 1, with the following rewritten paragraph:

The upper stacked chip scale package 150 has the same structure as the lower stacked chip scale package 110 except that solder balls are not formed on the ball land pads 163. That is to say, the upper stacked chip scale package 150 is a land grid array type package that includes semiconductor chip 151 attached to an upper surface of the substrate 161 with adhesive 171. A plurality of bonding pads 152 on semiconductor chip 151 are electrically connected to the circuit patterns 165 by bonding wires 175 passing through a hole 167 formed in the central area of the substrate 161. In this embodiment, a center pad type semiconductor chip 151, which has bonding pads formed on the central region of the chip, is preferred. The bonding wires 175, bonding pads 152 and circuit patterns 165 are protected by the encapsulating part 183.